

DOCKET NO. FIS9-2003-0238US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Haining S. Yang, *et. al.*

Group Art Unit: Unknown

Serial No.: 10/707,842

Examiner: unknown

Filed: 01/16/2004

For: **METHOD AND APPARATUS TO INCREASE STRAIN EFFECT IN A TRANSISTOR CHANNEL**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.56**

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application. A copy of the non-US patent documents is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that these documents be considered by the Examiner and formally made of record in this application.

Respectfully submitted,

Andrew M. Calderon
Reg. No. 38,093

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McLean, VA 22102
(703)712-5000

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FORM PTO-1449 (Modified)	ATTY. DOCKET NO. FIS9-2003-0238US1	SERIAL NO. 10/707,842
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Haining S. Yang, et al.	
(Use several sheets if necessary)	FILING DATE: 01/16/2004	GROUP: Unassigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6,228,694 B1	5/8/2001	Doyle et al.			
	6,406,973 B1	6/18/2002	Lee			
	6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
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	5,310,446	5/10/94	Konishi et al.			
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	US 2002/0090791 A1	7/11/2002	Doyle et al.			
	US 2002/0074598 A1	6/20/2002	Doyle et al.			
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	6,521,964 B1	2/18/2003	Jan et al.			
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FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

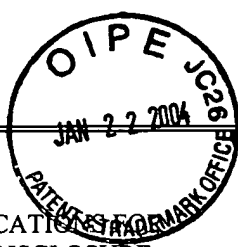
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	5,081,513	1/14/1992	Jackson, et al.			
	3,602,841	8/31/1971	McGroddy			
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	6,046,464	4/4/2000	Schetzina			
	6,025,280	2/15/2000	Brady, et al.			

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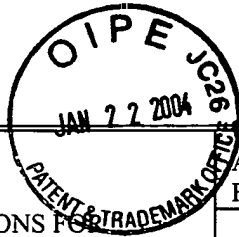
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	5,940,736	8/17/1999	Brady, et al.			
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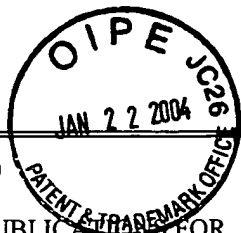
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	5,557,122	9/17/1996	Shrivastava, et al.			
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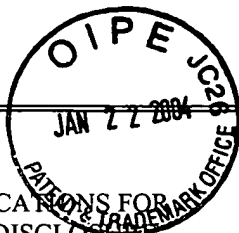
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		Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
		Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
		Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
		F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
		Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
		A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
		K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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